APPLICATION BRIEF

A Workflow Combining Ansys Sherlock, Icepak, and Mechanical to Evaluate the Reliability of Electronic Systems in Autonomous Vehicles

This workflow shows how Ansys Sherlock, Ansys Icepak, Ansys HFSS and Ansys Mechanical can be used to mitigate certain failure risks of printed circuit board assemblies (PCBA) within an autonomous vehicle.

We will explain the workflow using a hypothetical project involving a printed circuit board assembly (PCBA) mounted on top of a vehicle in an aluminum chassis within a larger housing. In this outline, we will use the Intel Galileo board, an open-source PCBA.

Additional assumptions:

- Natural and forced air convection is investigated
- Driverless taxi application
- Vehicle is assumed to be on for approximately 15 hours per day, everyday
- Residential roads
- Frequent potholes

/ Workflow:

1. We will begin with model initiation within Sherlock. Sherlock allows for the rapid creation of models utilizing electronic computer-aided design (ECAD) files and has important defeaturing options that assist in moving from ECAD to a computer-aided design (CAD) model to a usable finite element analysis (FEA) or computational fluid dynamics (CFD) model.

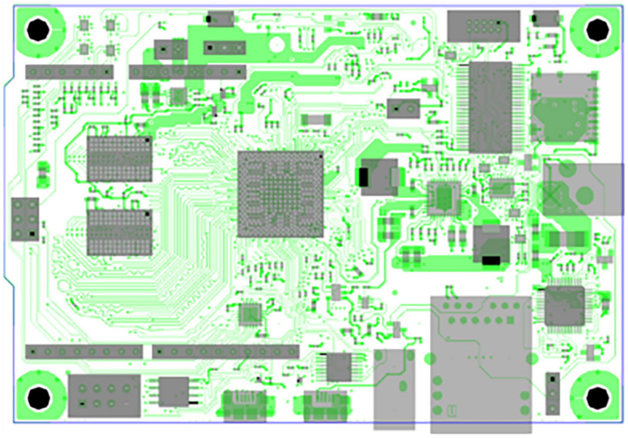
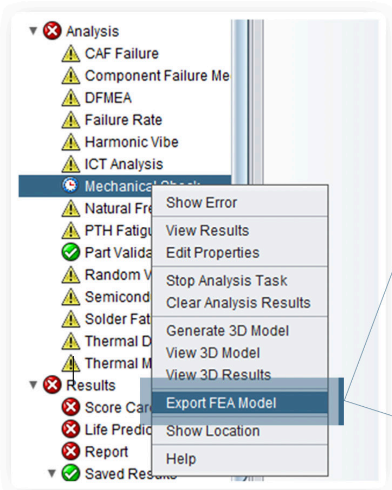


Figure 1: 2D Layer View of the PCBA in Sherlock.

2. Once you have built a PCBA in Sherlock, it can be exported directly into Workbench. Sherlock automates a variety of functions to facilitate the creation of a functional FEA model, including part size filtering, enabling/disabling of component leads, body faceting for easy meshing, and creation and assignment of material properties.



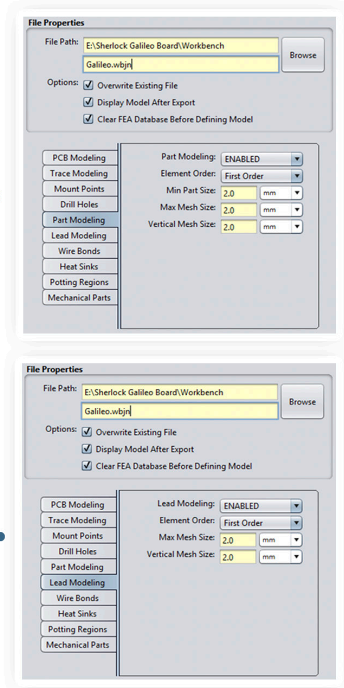


Figure 2: Sherlock Model Export Interface.

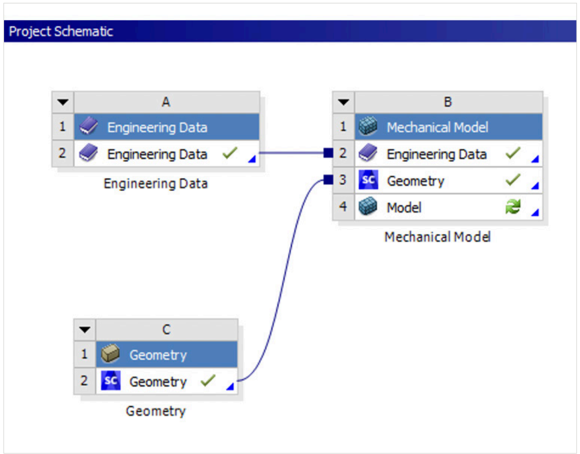


Figure 3: Workbench View of the Exported Model.

3. With a model of the PCBA now in Workbench, you are free to make changes to the geometry, such as adding housings or other structural details. It is sometimes advisable to create a copy of the model, so that different versions of the model can be used in Icepak and Mechanical. Sometimes, because the meshing and solving is done differently in CFD vs. FEA, it is preferable to have minor geometric differences depending on which tool is being used.

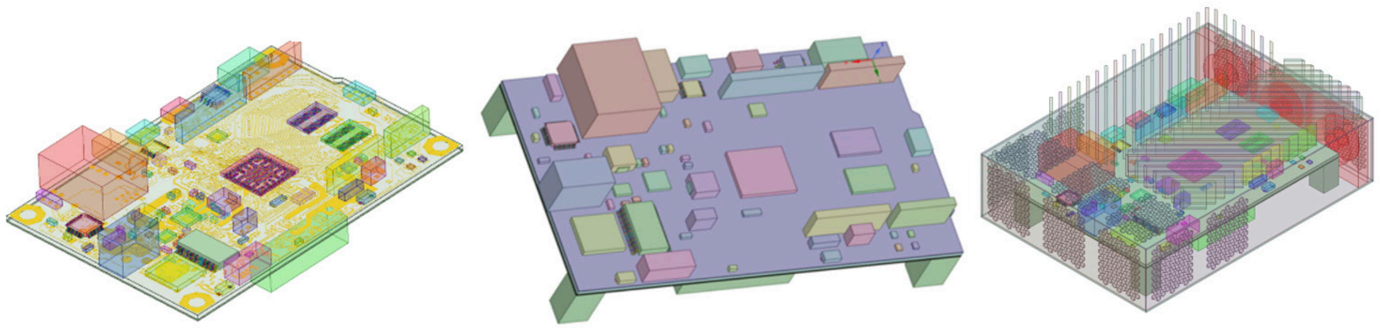


Figure 4: PCBA Geometry from Sherlock (top left) and PCBA after Housing is added in Spaceclaim.

4. In this analysis, we use Ansys Electronics Desktop (AEDT) to conduct two Icepak/HFSS iterative PCBA temperature analyses:

- Natural Convection only.
- Forced convection with three 3.0 CFM fans.

Power dissipations are applied on several critical components and 20˚C ambient air within the larger box is assumed.

5. Icepak is used to calculate temperature gradients throughout the PCBA; however, it does not account for power losses inside the PCB, which can sometimes result in significant temperature rises. The Ansys HFSS 3D layout tool is used to calculate temperature dependent losses inside the PCB.

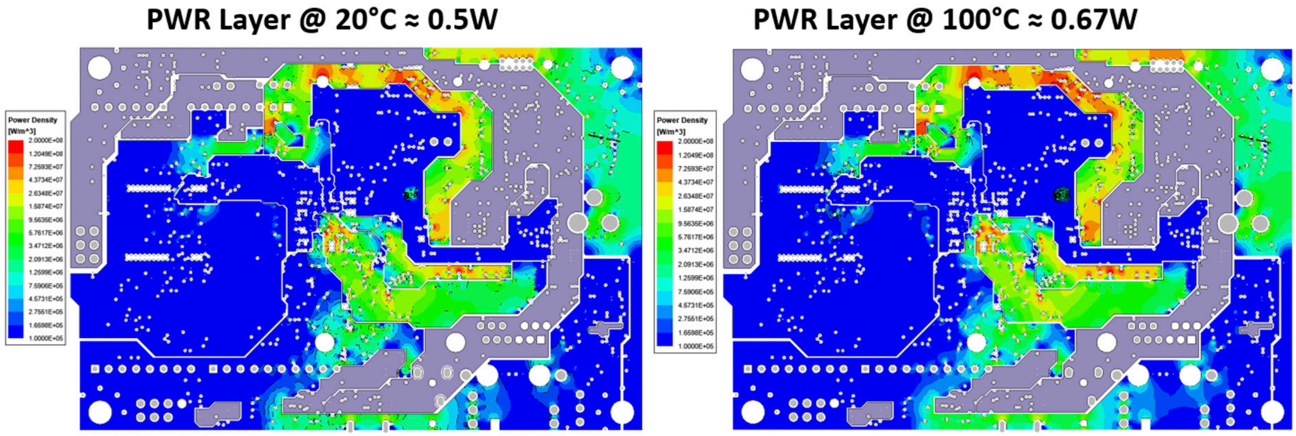


Figure 5: HFSS Computed DCIR Losses.

6. These losses are then mapped as heat loads in Ansys Icepak and coupled to the thermal solution to more accurately calculate board temperature gradients for both the forced and natural convection conditions. Thermal and PCBA reliability results with and without the inclusion of the HFSS DCIR analysis are presented here to show their potential significance.

As shown in the results below, the DCIR losses are due to current crowding, which can increase hotspot temperatures on the PCB:

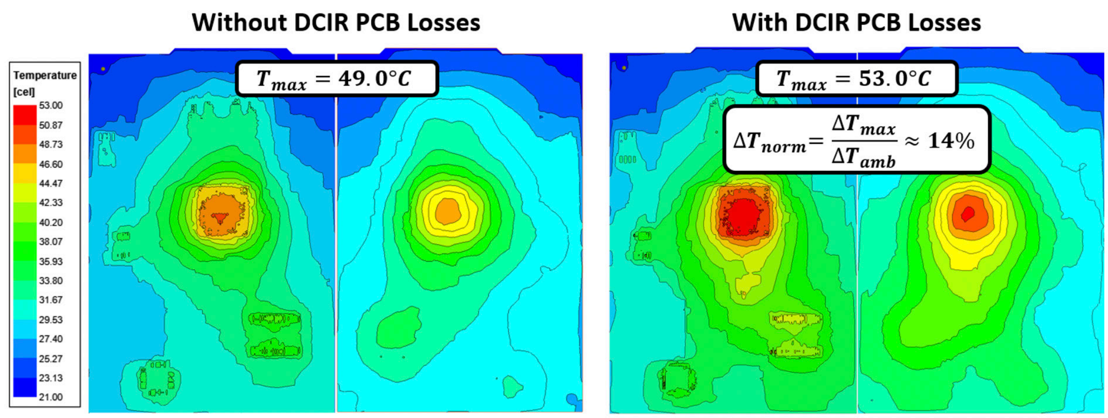


Figure 6: Natural Convection Icepak Thermal Gradient Results.

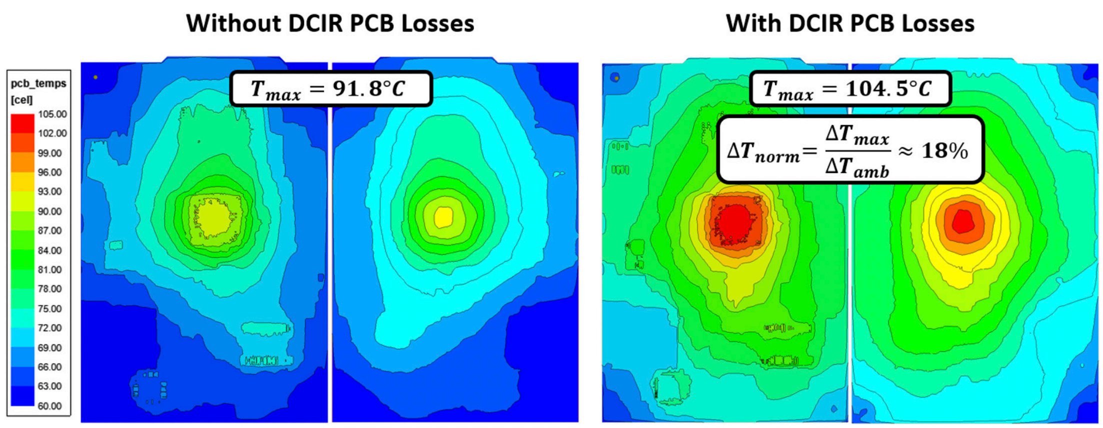


Figure 7: Natural Convection Icepak Thermal Gradient Results.

7. The resulting thermal maps can be imported back into Sherlock to quantify the solder fatigue failure risk associated with power cycling. The profile here assumes one power cycle per day, resulting in one large temperature swing.

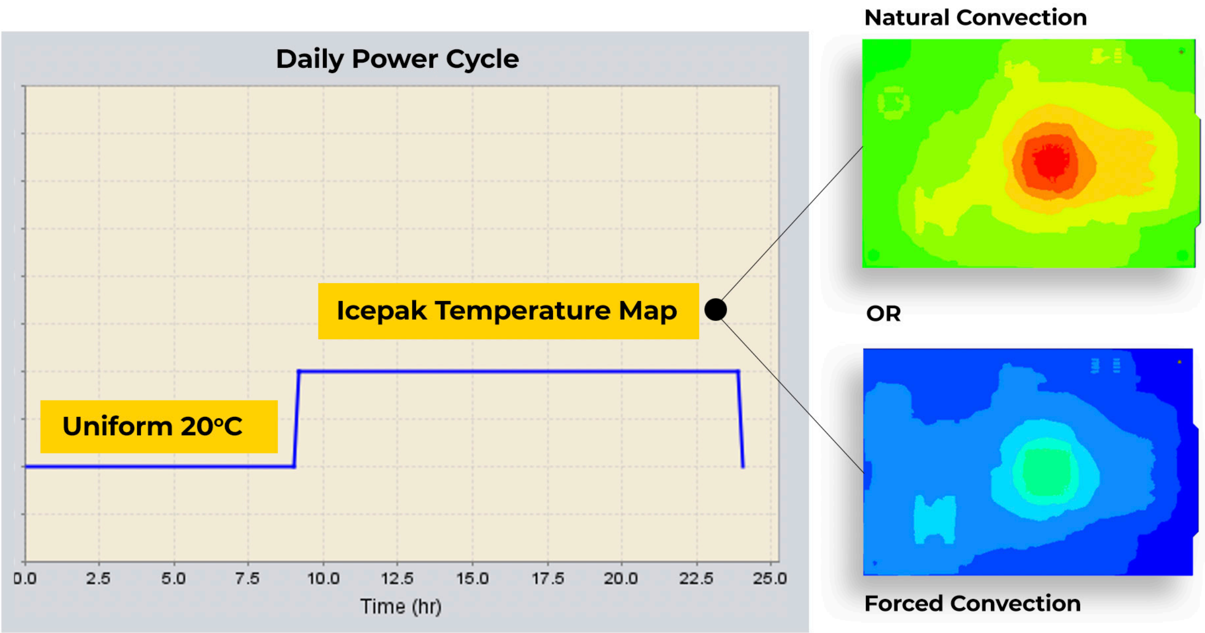


Figure 8: Sherlock Thermal Cycle.

8. The Sherlock analysis shows a solder fatigue risk resulting from the temperature swings when the board heats up and cools down during daily power cycling:

All Component Pass Natural Convection without DCIR

RefDes	Package	Part Type	Model	Side	Material	Solder	Max dT (C)	Damage	TTF (years)	Cycles To Fail	Score
U2A5	CBGA-393	IC	CBGA	TOP	LAMINATE-BGA	SAC305	69.3	3.0E-1	6.58	2,405	2.6
U1B5	BGA-78	IC	BGA	TOP	LAMINATE-BGA	SAC305	56.2	1.6E-1	12.22	4,463	10.0
U1A1	BGA-78	IC	BGA	TOP	LAMINATE-BGA	SAC305	55.6	1.6E-1	12.58	4,595	10.0
Y3L1	0000	OSCILLATOR	CC	BOT	ALUMINA	SAC305	57.5	1.0E-1	19.37	7,073	10.0
Y2A1	0000	OSCILLATOR	CC	TOP	ALUMINA	SAC305	56.1	3.7E-2	>20	19,510	10.0
U2L1	BGA8	IC	BGA	BOT	SILICON	SAC305	58.4	3.3E-2	>20	22,401	10.0
U2M1	BGA8	IC	BGA	BOT	SILICON	SAC305	57.8	3.2E-2	>20	23,160	10.0

Some Components Fail Natural Convection with DCIR

RefDes	Package	Part Type	Model	Side	Material	Solder	Max dT (C)	Damage	TTF (years)	Cycles To Fail	Score
U2A5	CBGA-393	IC	CBGA	TOP	LAMINATE-BGA	SAC305	81.7	5.1E-1	3.92	1,430	0.0
U1B5	BGA-78	IC	BGA	TOP	LAMINATE-BGA	SAC305	63.7	2.4E-1	8.35	3,048	5.6
U1A1	BGA-78	IC	BGA	TOP	LAMINATE-BGA	SAC305	63.6	2.4E-1	8.40	3,068	5.7
Y3L1	0000	OSCILLATOR	CC	BOT	ALUMINA	SAC305	67.4	1.6E-1	12.30	4,493	10.0
Y2A1	0000	OSCILLATOR	CC	TOP	ALUMINA	SAC305	69.8	7.0E-2	>20	10,495	10.0
U2L1	BGA8	IC	BGA	BOT	SILICON	SAC305	70.5	5.8E-2	>20	12,646	10.0
U2M1	BGA8	IC	BGA	BOT	SILICON	SAC305	70.5	5.8E-2	>20	12,646	10.0

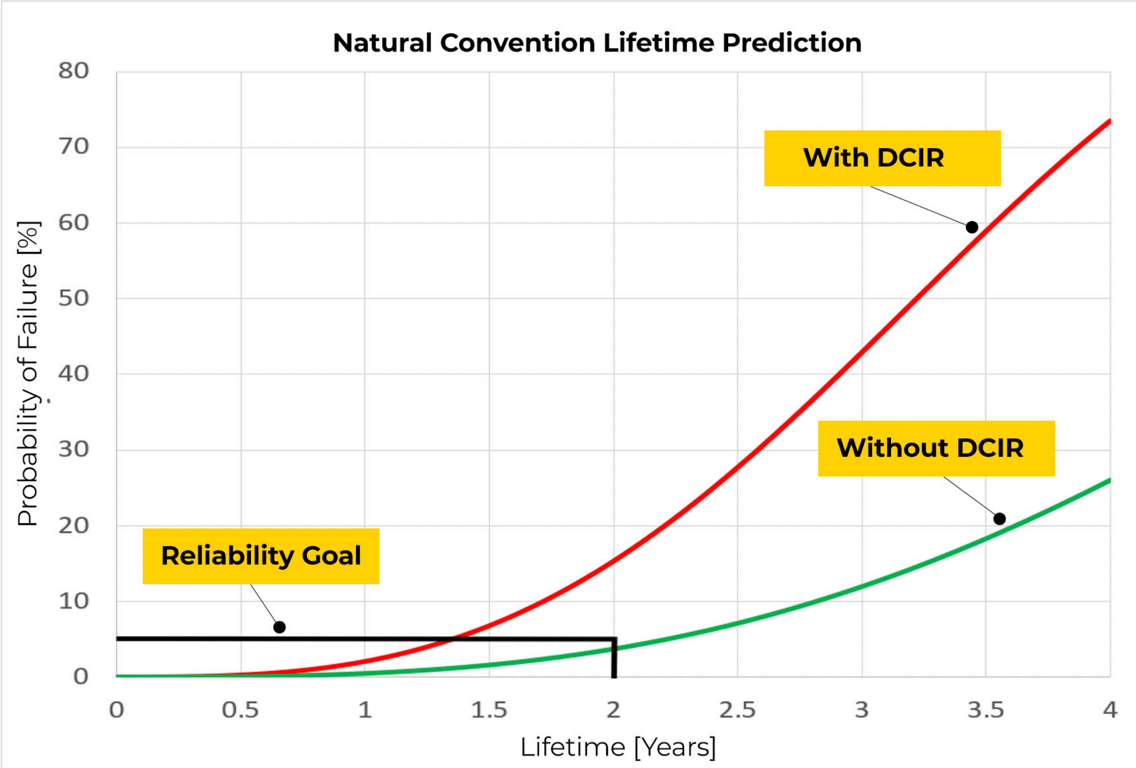


Figure 9: Natural Convection Sherlock Solder Fatigue Results

The results show that without fans included in the housing, the Icepak-only analysis indicates that the PCBA will meet its reliability goals under the analyzed loading and duty cycle, albeit with slim margin.

However, when the DCIR losses are included, the additional heating results in the PCBA missing its reliability goal by highlighting the large BGA at the center of the board as a failure risk. This is a potential failure risk that may not have been properly identified without the incorporation of HFSS in this workflow.

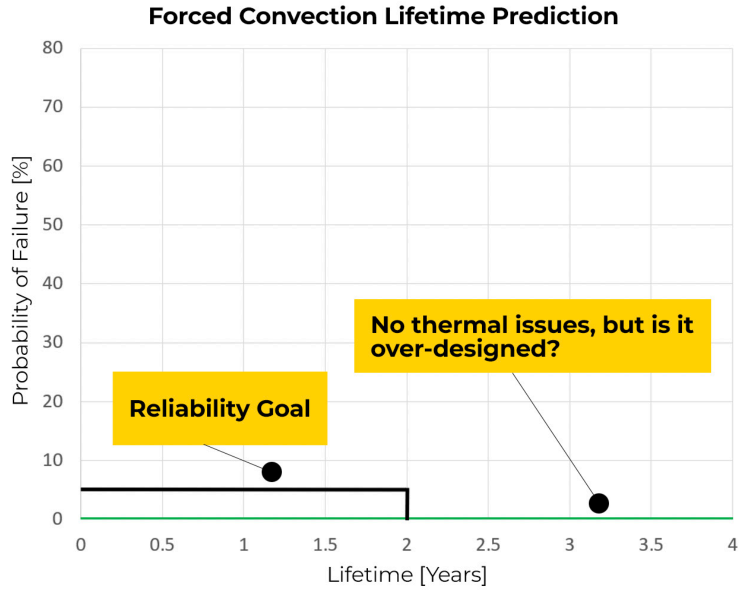
9. These results indicate that the natural convection solution will likely not be adequate for this use case, so the reliability of the forced convection solution was next investigated.

All Components Pass Forced Convection without DCIR

RefDes	Package	Part Type	Model	Side	Material	Solder	Max dT (C)	Damage	TTF (years)	Cycles To Fail	Score
U2A5	CBGA-393	IC	CBGA	TOP	LAMINATE-BGA	SAC305	26.7	2.1E-2	>20	35,283	10.0
Y3L1	0000	OSCILLATOR	CC	BOT	ALUMINA	SAC305	15.0	3.9E-3	>20	187,992	10.0
U1A1	BGA-78	IC	BGA	TOP	LAMINATE-BGA	SAC305	11.9	3.1E-3	>20	239,042	10.0
U1B5	BGA-78	IC	BGA	TOP	LAMINATE-BGA	SAC305	11.8	3.0E-3	>20	243,298	10.0
Y2A1	0000	OSCILLATOR	CC	TOP	ALUMINA	SAC305	16.6	1.9E-3	>20	390,344	10.0
U2L1	BGA8	IC	BGA	BOT	SILICON	SAC305	18.8	1.6E-3	>20	462,058	10.0
U2M1	BGA8	IC	BGA	BOT	SILICON	SAC305	18.1	1.4E-3	>20	505,566	10.0
F4B1	0000	FUSE	CC	TOP	ALUMINA	SAC305	11.0	1.2E-3	>20	592,831	10.0

All Components Pass Forced Convection with DCIR

RefDes	Package	Part Type	Model	Side	Material	Solder	Max dT (C)	Damage	TTF (years)	Cycles To Fail	Score
U2A5	CBGA-393	IC	CBGA	TOP	LAMINATE-BGA	SAC305	30.3	2.9E-2	>20	25,497	10.0
Y3L1	0000	OSCILLATOR	CC	BOT	ALUMINA	SAC305	17.3	5.4E-3	>20	136,176	10.0
U1A1	BGA-78	IC	BGA	TOP	LAMINATE-BGA	SAC305	12.6	3.5E-3	>20	208,528	10.0
U1B5	BGA-78	IC	BGA	TOP	LAMINATE-BGA	SAC305	12.3	3.3E-3	>20	221,745	10.0
U2L1	BGA8	IC	BGA	BOT	SILICON	SAC305	23.4	2.7E-3	>20	268,565	10.0
U2M1	BGA8	IC	BGA	BOT	SILICON	SAC305	23.4	2.7E-3	>20	268,565	10.0
Y2A1	0000	OSCILLATOR	CC	TOP	ALUMINA	SAC305	19.1	2.6E-3	>20	282,218	10.0
U3A1	QFN-40 (MO-208HHEA-H)	IC	QFN	TOP	OVERMOLD-QFN	SAC305	20.0	2.2E-3	>20	335,752	10.0



10. With fans included in the design, the reliability goal for the PCBA is met with significant margin regardless of the incorporation of DCIR analysis in the workflow. The fan solution would prevent solder fatigue, but it is possibly over-designed. These results hint that a compromise may be achieved. Perhaps a heat sink attached to the high power BGA at the center of the board that is driving peak temperature would reduce temperatures enough to prevent failure risk even without the fans.

    For the remainder of this analysis, we will assume we move forward with the forced air solutions. This would prevent thermal cycling related solder fatigue, but would it fully mitigate failure risk associated with temperature.

11. In order to fully capture the effects of part temperature rise, the Icepak CFD results must be included as an input to the structural FEA analysis. This is imperative to properly account for constraint effects from the PCBA expanding within its housing and buckling/warping, temperature gradients resulting in mismatched component/board expansion rates, and temperature-dependent material properties.

12. To accomplish this, the temperature map with airflow is imported into Ansys Mechanical ahead of a pothole shock simulation.

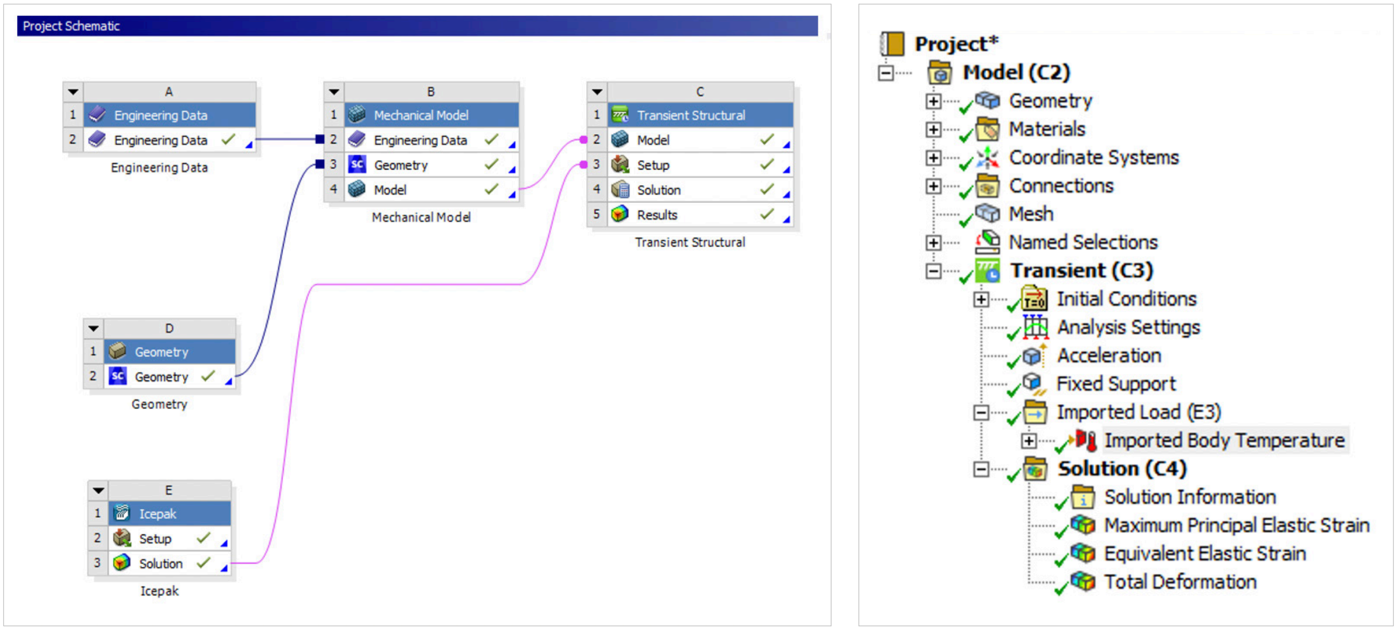


Figure 10: Mapping of Thermal Gradients from Icepak to Mechanical.

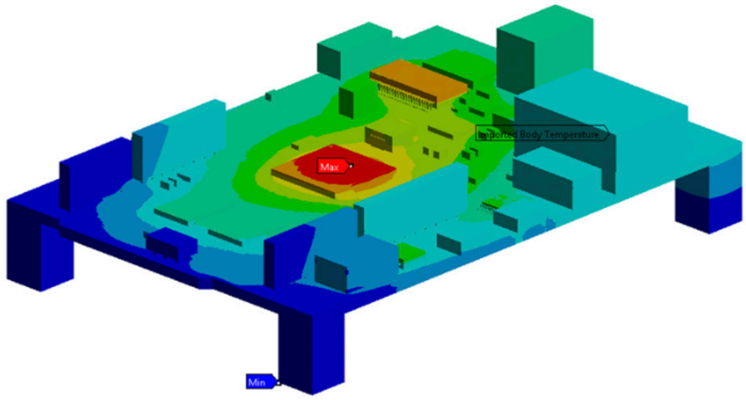


Figure 11: Thermal Gradients in Mechanical.

13. We run an FEA analysis to quantify the effect of the PCBA being stressed when the vehicle encounters a pothole. The simulation was conducted assuming the PCBA was operational, so the thermal gradient was first incorporated as a pre-load prior to the pothole shock load application.

    The loading from the pothole was approximated with a 25G, 10ms half-sine pulse applied in the negative out-of-plane direction.

    The resulting peak PCBA strains are shown below.

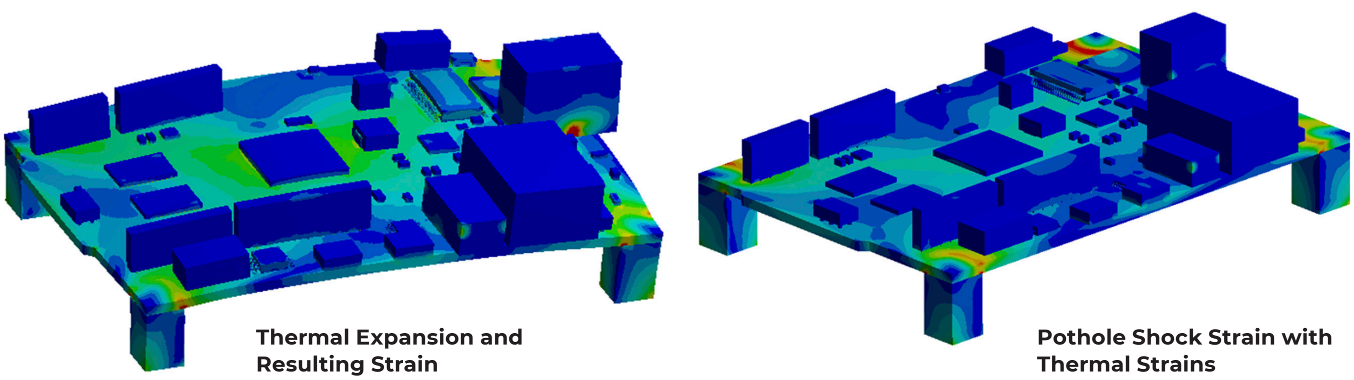


Figure 12: Mechanical Pothole Shock Results.

14. The FEA results from Mechanical are then imported to Sherlock, and the strains are used to predict reliability (probability of failure).

Again, our hypothesis is that the autonomous vehicles will hit 3 potholes per hour, while operating 15 hours per day for 2 years. In this analysis, even with the inclusion of the thermal expansion strains, none of the components are predicted to be failure risks. The Galileo board is a relatively small, thick PCB, making it stand up fairly well to shock events.

RefDes	Package	Part Type	Side	Max Disp	Max Strain	TTF (years)	Failure Prob	Failure Prob / Cycle
U2A5	CBGA-393	IC	TOP	4.6E-2	3.0E-4	>20	0.4	8.2E-6
J1B2	BOX CONN	PLUG CONNECTOR	TOP	1.7E-2	3.5E-4	>20	0.3	6.2E-6
J4B1	BOX CONN	JACK	TOP	3.9E-2	2.1E-4	>20	0.1	1.6E-6
U1A1	BGA-78	IC	TOP	2.7E-2	1.3E-4	>20	0.0	5.9E-7
S1	SON SW	SWITCH	TOP	1.3E-2	3.9E-4	>20	0.0	3.1E-7
L2M1	C-BEND	INDUCTOR	BOT	4.4E-2	2.4E-4	>20	0.0	3.0E-7
U8	SSOP-48 (MO-118...	IC	TOP	3.5E-2	1.7E-4	>20	0.0	2.8E-7
U1B5	BGA-78	IC	TOP	2.8E-2	1.2E-4	>20	0.0	2.6E-7
U2L1	BGA8	IC	BOT	4.6E-2	2.9E-4	>20	0.0	1.5E-7
U2M1	BGA8	IC	BOT	4.6E-2	2.6E-4	>20	0.0	7.9E-8
J2	SIP CONN	PLUG CONNECTOR	TOP	1.0E-2	2.7E-4	>20	0.0	7.0E-8
Q1	SOT-23 (TO-236AB)	TRANSISTOR	TOP	9.5E-3	3.2E-4	>20	0.0	5.0E-8
L3A1	C-BEND	INDUCTOR	TOP	4.5E-2	1.7E-4	>20	0.0	2.4E-8
Y3L1	0000	OSCILLATOR	BOT	4.3E-2	2.1E-4	>20	0.0	6.9E-9
U6	SON	IC	TOP	9.5E-3	3.3E-4	>20	0.0	3.8E-9
U3A1	QFN-40 (MO-208H...	IC	TOP	4.0E-2	1.7E-4	>20	0.0	2.3E-9
C3A18	0603	CAPACITOR	TOP	4.1E-2	1.6E-4	>20	0.0	3.3E-12
C3A19	0603	CAPACITOR	TOP	4.2E-2	1.5E-4	>20	0.0	2.5E-12
C3A10	0402	CAPACITOR	TOP	4.5E-2	1.3E-4	>20	0.0	1.1E-13
C3A11	0402	CAPACITOR	TOP	3.9E-2	1.3E-4	>20	0.0	1.2E-13

Summary

The workflow outlined here highlights how incorporating thermal simulation, electrical simulation, mechanical simulation, and reliability physics during the design phase can provide significant information about the expected reliability behavior of an electronic product.

This Multiphysics workflow also opens the door for the incorporation of additional simulation tools to further refine the reliability predictions, such as digital twin workflows to analyze predicted reliability in real-time for specific fielded components.

It should also be noted that, because this is a hypothetical analysis, certain potentially significant conservative assumptions were made regarding component inputs, such as component and PCBA material properties. As a result, these predictions may not reflect the exact reliability behavior of the Galileo board in these conditions. A potential next step in this analysis after some design decisions are made could be to refine simulations and resulting reliability predictions with material testing.

ANSYS, Inc.
Southpointe
2600 Ansys Drive
Canonsburg, PA 15317
U.S.A.
724.746.3304
ansysinfo@ansys.com